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APPLICATION NO. FILING DATE		FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO	
10/087,744 03/05/2002		Glen Hush	M4065.0485/P485	7015	
24998	7590 05/15/2003				
DICKSTER	N SHAPIRO MORIN & C	EXAMINER			
2101 L STRI WASHINGT	EET NW OON, DC 20037-1526	LE, THONG QUOC			
			ART UNIT	PAPER NUMBER	
			2818		
			DATE MAILED: 05/15/2003		

Please find below and/or attached an Office communication concerning this application or proceeding.

<u> </u>			Applicati	on No	pplicant(s)	A
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	Offic Action Summary	Summany	10/087,744		HUSH ET AL.	
•	One Action	Summary	Examine		Art Unit	
	T. 444 WO DAT		Thong Q.		2818	
Peri d f		e or this communication	i appears on th	e cover sneet with	n the correspondence add	ress
THE I - Exter after - If the - If NO - Failu - Any I	MAILING DATE OF usions of time may be availal SIX (6) MONTHS from the network of reply specified period for reply is specified to reply within the set or e	above, the maximum statutory poxtended period for reply will, by sater than three months after the n	ON. FR 1.136(a). In no ev n. a reply within the sta eriod will apply and w statute, cause the app	ent, however, may a rep tutory minimum of thirty vill expire SIX (6) MONTI plication to become ABA	oly be timely filed (30) days will be considered timely. HS from the mailing date of this com NDONED (35 U.S.C. § 133).	nmunication.
Status	a patent term adjustment.					
1) 🗌	Responsive to con	nmunication(s) filed on	 •			
2a) <u></u> □	This action is FINA	AL . 2b)⊠	This action is	non-final.		
3)□ Dispositi		ion is in condition for al nce with the practice un			ers, prosecution as to the . 11, 453 O.G. 213.	merits is
4)⊠	Claim(s) 1-4,6-13,	16-21,24,27-32,35-41 a	and 44-50 is/are	e pending in the a	application.	
	4a) Of the above cla	aim(s) is/are with	ndrawn from co	nsideration.		
5)⊠	Claim(s) <u>1-4,6-13,1</u>	6-21, 24, 45-48 is/are	allowed.			
6)⊠	Claim(s) 27,36,49 a	and 50 is/are rejected.				
7)🖂	Claim(s) 28-32,35,3	<u>37-41 and 44</u> is/are obj	ected to.			
8)[Claim(s) are	subject to restriction a	nd/or election r	equirement.		
Applicati	on Papers					
	•	objected to by the Exar				
10)🛛	The drawing(s) filed	on <u>20 May 2002</u> is/are:	: a)⊠ accepted	or b) objected to	o by the Examiner.	
_	•	•			nce. See 37 CFR 1.85(a).	
11) 🔲 .		ng correction filed on _		•	sapproved by the Examiner	•
	• •	ed drawings are required	· -	ffice action.		
,—		ion is objected to by the	e Examiner.			
-	inder 35 U.S.C. §§					
• —	_	made of a claim for for	reign priority ur	nder 35 U.S.C. §	119(a)-(d) or (f).	
a)	☐ All b)☐ Some '	•				
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* 9	application	e certified copies of the on from the Internationa ailed Office action for a	il Bureau (PCT	Rule 17.2(a)).	eceived in this National S eceived.	tage
14) 🗌 A	.cknowledgment is r	nade of a claim for don	nestic priority u	nder 35 U.S.C. §	119(e) (to a provisional a	pplication
		of the foreign language made of a claim for don				
Attachmen	(s)					
2) Notic	e of References Cited (P e of Draftsperson's Pater nation Disclosure Statem	nt Drawing Review (PTO-948			ummary (PTO-413) Paper No(s) formal Patent Application (PTO-	

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DETAILED ACTION

1. Pre-amendment filed on November 22, 2002 has been entered.

2. Claims 1-4, 6-13,16-21,24, 27-32,35-41,44-50 are presented for examination.

Information Disclosure Statement

- This office acknowledges receipt of the following items from the Applicant:
 Information Disclosure Statement (IDS) filed on August 15 2002.

 Information Disclosure Statement (IDS) filed on September 26, 2002.
 Information Disclosure Statement (IDS) filed on November 22, 2002.
- 3. Information disclosed and list on PTO 1449 was considered.

Drawings

3. The corrected or substitute drawings were received on May 20, 2002. These drawings are acceptable.

Specification

4. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

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(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 27, 36 are rejected under 35 U.S.C. 102(b) as being anticipated by BuerGer, Jr. (Pub. U.S. Patent No. 2002/0050606).

Regarding claims 27, 36, Buerger, Jr. discloses a semiconductor memory structure (Figure 1) comprising:

a processor (it is inherent in any computer system, for example, Harshfield US Patent No. 5,818,749)

a column line (Figure 1, 4) and a row line (Figure 1, 5) associated with a programmable conductor random access memory cell;

a programmable conductor memory element (Figure 1, 2), a first terminal of which is coupled to the column line and a second terminal of which is coupled to a first of reverse connected diode pair (Figure 1, 3a, 3b), wherein a second side of reverse connected diode pair is coupled to the row line (Figure 1); and

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a sense amplifier (Column 4, paragraph 0057) for comparing a voltage on the column line with a reference voltage during read operation to determined a logic state of the programmable conductor memory element.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 49-50 are rejected under 35 U.S.C. 102(b) as being anticipated by Harshfield (U.S. Patent No. 5,818,749).

Regarding claims 49-50, Harshfield discloses a processor system comprising: a processor (Figure 2, 24, Column 1, lines 26-30); and

a semiconductor memory structure (Figure 2, 16) coupled to the processor, the semiconductor memory structure comprising:

a column line (Figure 3, 22) and row line (Figure 3, 20) associated with a programmable conductor random access memory cell (Figure 3, 18);

a programmable conductor memory element (Figure 4, 30), a first terminal of which is coupled to the column line and second terminal of which is coupled to a first terminal of a zener diode (Figure 4, 32), wherein

a second terminal of the zener diode is coupled to the row line (Figure 3); and a sense amplifier (Figure 10, 56) for comparing a voltage on the column line with a reference voltage during a read operation to determined a logical state of the programmable conductor memory element (Column 9, lines 25-35).

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Allowable Subject Matter

8. Claims 28-32, 35, 37-41, 44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 28-32, 35, 37-41, 44 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Buerger, Jr. (U.S. Patent No. 2002/0050606), Harshfield (U.S. Patent No. 5,818,749), and others, does not teach the claimed invention having precharge circuits respectively precharging the column line and row line to a common predetermined voltage level prior to the read operation.

9. Claims 1-4, 6-13, 16-21, 24, 45-48 are allowed.

Claims 1-4, 6-13, 16-21, 24, 45-48 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Buerger, Jr. (U.S. Patent No. 2002/0050606), Harshfield (U.S. Patent No. 5,818,749), and others, does not teach the claimed invention having a method of sensing a stored value of a programmable conductor random access memory element including setting the row line and the column line to a common voltage level.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 703-306-9123. The examiner can normally be reached on 8:00am-5:00pm M-F.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 703-308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3329.

Thong Q. Le Examiner Art Unit 2818

May 9, 2003